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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,968	01/22/2002	Yaniv Avital	12410.0016	7889

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EXAMINER	
JOSEPH, JAISON	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,968	AVITAL ET AL.	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6, 10, 11, 13, 14, 16 -20, 23, 26-28, 29-31, and 33-34* is/are rejected.

7)☒ Claim(s) *5, 7- 9, 12, 15, 21, 22, 24, 25, and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Regarding claim 29, the phrase "The method according to claim 24" renders the claim indefinite because a method claim depend on an apparatus claim. The claim 24 is an apparatus claim.

Regarding claim 30, the phrase "The method according to claim 24" renders the claim indefinite because a method claim depend on an apparatus claim. The claim 24 is an apparatus claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 – 4, 18 – 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imaizumi et al. (US Patent 6,707,844 B1) in view of Cantwell (US Patent 5,117,232).

Regarding claim 1, Imaizumi et al. teach a correlator having a sample register to store and output input samples every chip period of an input sample stream clocked at an over sampling ratio of R times a nominal sampling clock rate (see column 2, lines 29 – 33) , a code register adapted to store and output a code value at nominal sampling clock rate (see column 3, line 39 – 42), a multiplier coupled to said sample register and said code register, said multiplier adapted to multiply the output of said sample register with the output of said code register (see column 2, lines 34 – 37), Imaizumi et al. failed to teach a adder adapted to add the output of said multiplier with the correlation sum output of the last stage of an M-stage integration result shift register and to produce a correlation sum therefrom; said integration results shift register adapted to store m correlation sums wherein correlation sums output of said adder are shifted into said integration results shift register at said over sampling clock rate such that the over sampling phase of the correlation sum at the output of said integration results shift register corresponds to the correlation sum currently at the input to said adder. However, Cantwell teaches an adder 68 adapted to add the output of said multiplier with the correlation sum output of the last stage of an M-stage integration result shift register 69 and to produce a correlation sum therefrom, said integration results shift register adapted to store M correlation sums wherein correlation sums output of said adder are shifted into said integration results shift register at said over sampling clock rate such

that the over sampling phase of the correlation sum at the output of said integration results shift register corresponds to the correlation sum currently at the input to said adder (see figure 6). Therefor it would be obvious to an ordinary skilled in the art at the time the invention was made to use Cantwell's Integrator in Imaizumi et al.'s correlator to provide a GPS which performs N-bit correlation of received PN code modulated carrier using minimum circuits and interconnections to facilitate very large scale integrated circuit implementation (see column 2, lines 44 – 48).

Regarding claim 2, which inherits the limitations of claim 1, Imaizumi et al. teach said code register is loaded with new code value every over sampling period (see column 3, lines 10 – 13).

Regarding claim 3, which inherits the limitations of claim 1, Imaizumi et al. further teach said code register is loaded with code values output by a code generator (see column 3, lines 10 – 13).

Regarding claim 4, which inherits the limitations of claim 1, Cantwell teach said sample register, said code register, said multiplier, said adder and said integration result shift register are adapted to process and output complex values (see figure 3).

Regarding claim 18, Cantwell teaches a result register 71 coupled to the output of the last stage of said integration results shift register and adapted to sequentially store final correlation sums output (see figure 6)

Regarding claim 19, Cantwell teaches a timing means 20 adapted to provide suitable timing control and clock signals to the correlator (see figure 2).

Regarding claim 20, Cantwell teaches a means 164 for zeroing out each individual correlation sum when integration is complete (see figure 11A).

Regarding claim 23, Cantwell teaches a means for simultaneously outputting and storing a final correlation sum sequentially in a results register and zeroing out each individual correlation sum when integration is complete.

Claims 6, 10, 11, 13, 14, 28, 31, are rejected under 35 U.S.C. 103(a) as being unpatentable over over Imaizumi et al. (US Patent 6,707,844 B1) in view of Cantwell (US Patent 5,117,232) as applied to claim 1 above, and further in view of Hakala (US Patent 6,539,048).

Regarding claim 6, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 1 is applicable hereto. Imaizumi and Hakala failed to teach the code register is circular code shift register. However Hakala teaches a circular code shift register in CDMA code generator (see column 4, lines 64 – 66). Therefor it would be obvious to an ordinary skilled in the art at the time the invention was made to use a circular shift register in Imaizumi et al.'s code generator to provide an improved matched filter that exhibits a reduced power consumption (see column 2, lines 35 – 37).

Regarding claim 10, which inherits the limitations of claim 6, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 4 is applicable hereto.

Regarding claim 11, which inherits the limitations of claim 6, Hakala teaches said code shift register is adapted to e parallel loaded with N code values once every input sample interval (see column 5, lines 27 – 28).

Regarding claim 13, which inherits the limitations of claim 11 or 12, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 3 is applicable hereto.

Regarding claim 14, which inherits the limitations of claim 6, Cantwell teaches an integration result shift register comprises plurality of registers and selection means arranged such that a one orr more said plurality of registers are selectably configured in accordance with a length selection signal to receive and store correlation sums output from the adder and to function as a shift register (see figure 6).

Regarding claim 28, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 6 is applicable hereto.

Regarding claim 31, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 6 is applicable hereto.

Claims16 and 17 arerejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US Patent 6,005,889) in view of Imaizumi et al. (US Patent 6,707,844 B1), Cantwell (US Patent 5,117,232) and Hakala (US Patent 6,539,048).

Regarding claim 16, Chung et al teach a receiver having a radio frequency front end (see abstract) for receiveing a spread spectrum RF signal having a plurality of multipath components, a searcher (figure 2, component 217) adapted to measure the multipath components of said RF signal and to generate one or more path selections

and a collapse filter (see abstract) bank for generating a plurality of demodulated signals from said RF signal. Chung et al. failed to teach a sample register adapted to store and output input samples at a first clock rate; an N-stage circular code shift register adapted to store N code values and clocked at a second clock rate; a multiplier coupled to said sample register and said code shift register, said multiplier for multiplying input samples with the code value output of the last stage of said code shift register, wherein said code shift register is circularly shifted such that each input sample is sequentially multiplied by each of N codes; an adder adapted to add the output of said multiplier with the correlation sum output of the last stage of an M-stage integration result shift register and to produce a correlation sum therefrom; said integration results shift register adapted to store M correlation sums wherein correlation sums output of said adder are shifted into said integration results shift register at said second clock rate such that the correlation sum at the output of said integration results shift register corresponds to that of the correlation sum currently at the input to said adder; a results register adapted to store final correlation sums output of said integration results register and to output said final correlation sums as demodulated signals; However, of Imaizumi et al., Cantwell and Hakala meet these limitations as explained in the above rejection of claim 6. Thereforeit would be obvious to an ordinary skilled in the art art at the time the invention was made to combine the teachings of Chung et al., Imaizumi et al., Cantwell and Hakala to to provide a method and system for detecting frequency offsets in a PN signal with decreased detection times (see column 3, lines 26 – 28).

Regarding claim 17, which inherits the limitations of claim 16, Chung et al further teaches a channel decoder adapted to decode said received data input signal to generate a decoded output signal (see figure 2).

Claims 26, 27, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imaizumi et al. (US Patent 6,707,844 B1) in view of Cantwell (US Patent 5,117,232) and Hakala (US Patent 6,539,048) as applied to claim 1 above, and further in view of Wang et al. (US Patent 6,501,788).

Regarding claim 26, which inherits the limitations of claim 1, 6, or 16, Imaizumi et al, Cantwell and Hakala failed to teach the correlator is adapted to implemented in an Application Specific Integrated Circuit. However Wang et al. teaches the correlator can be in an Application Specific Integrated Circuit (see column 9, lines 27 – 38). Therefore, it would be obvious to an ordinary skilled in the art at the time the invention was made to implement the correlator in Application Specific Integrated Circuit to provide communications apparatus and methods that can reduce multi-user interference in spread-spectrum communications systems (see column 3, lines 36 – 39).

Regarding claim 27, which inherits the limitations of claim 1, 6, or 16, Imaizumi et al, Cantwell and Hakala failed to teach the correlator is adapted to implement in a Field Programmable Gate Array. However Wang et al. teaches the correlator can be in a Field Programmable Gate Array (see column 9, lines 27 – 38). Therefore, it would be obvious to an ordinary skilled in the art at the time the invention was made to implement the correlator in a Field Programmable Gate Array to provide communications

apparatus and methods that can reduce multi-user interference in spread-spectrum communications systems (see column 3, lines 36 – 39).

Regarding claim 33, which inherits the limitations of claim 31, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 26 is applicable hereto.

Regarding claim 34, which inherits the limitations of claim 31, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 27 is applicable hereto.

Allowable Subject Matter

Claims 5, 7, 8, 9, 12, 15, 21, 22, 24, 25, and 32 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
04/18/2005

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